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## Electronic noise in charge sensitive preamplifiers for X-ray spectroscopy and the benefits of a SiC input JFET



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### ABSTRACT

A comprehensive summary and analysis of the electronic noise affecting the resolution of X-ray,  $\gamma$ -ray and particle counting spectroscopic systems which employ semiconductor detectors and charge sensitive preamplifiers is presented. The noise arising from the input transistor of the preamplifier and its contribution to the total noise is examined. A model for computing the noise arising from the front-end transistor is also presented and theoretical calculations comparing the noise contribution of transistors made of different materials are discussed, emphasizing the advantages of wide bandgap transistor technology.

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### 1. Introduction

A typical detection system for X-ray,  $\gamma$ -ray or particle counting spectroscopy with a photodiode consists of the detector, the preamplifier, the main shaping amplifier and the multichannel analyzer (MCA) [1]. Each of these introduces noise. The detector sets the fundamental statistical limit to the resolution of the system with the, so called, Fano noise [2]. This is related to the statistical nature of the ionization process. The movement of the charge inside the detector also introduces noise, caused by impurities and defects of the material resulting in charge trapping [3]. The third source of noise arises from electronics. The characteristic parameters of the detector, the input transistor of the preamplifier circuit and the filtering are all involved in the electronics noise. The signal of the detector is supplied to the input transistor of the preamplifier and it is this first stage whose noise plays the most important role.

Although other researchers have worked on the noise analysis of the input transistor for low noise X-ray charge sensitive preamplifiers (including very notably work reported in Ref. [4]), in this paper we present a comprehensive overview of the noise components, focusing on those arising from the input transistor in a feedback resistorless charge sensitive preamplifier, together with theoretical calculations relating the primary characteristics of the input transistor (including its material and geometry) to its noise components. We calculate and theoretically demonstrate the

benefits of using a wide bandgap (SiC) JFET rather than a comparable Si JFET, in order to inform the future development of X-ray spectroscopy preamplifiers for use in high temperature applications, such as space missions to the surfaces of Mercury or Venus, or to potential hot hydrothermal vents in the oceans of Europa [5].

Input transistors for X-ray spectroscopy preamplifiers are often chosen to be JFETs [6–9]. JFETs have lower noise compared to MOSFETs which results in better energy resolution [2,10,11]. This can be attributed to JFETs having a lower  $1/f$  noise [11]. Consequently, in the present work we restrict our discussion solely to JFETs. However, MOSFETs can be used in high density CMOS integrated circuits where JFETs cannot be employed [12]. Study of SiC MOSFETs for preamplifier applications potentially using transistor models such as BSIM [13] and PSP [14] would be valuable but is not included in the present work.

The noise components that constitute the electronics noise are described in Section 2. This is done by explaining the different phenomena which generate each noise component and their quantitative contribution to the overall noise in terms of their equivalent noise charge. In Section 3, the parameters of the input JFET and their effect on the total noise of the system are examined. In Section 4, calculations and comparison between the noise contribution arising from the same geometry JFET made of Si and SiC are presented.

### 2. Introduction to noise components

There are five main components which constitute the electronics noise of the system. These are the series white noise, the

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parallel white noise, the  $1/f$  series noise, the dielectric noise and the induced gate current noise as they are analyzed by Bertuccio et al. [4]. In this section, these sources are introduced in turn. The contribution of the FET is subsequently discussed in Section 3.

### 2.1. Series white noise

The series white noise (voltage noise) arises from the thermal noise of the current flowing at the channel of the input JFET. The equivalent noise charge (ENC) in  $e^-$  rms for the white series noise is given by Ref. [4] as:

$$ENC_{ws} = \frac{1}{q} \sqrt{\frac{A_1}{2} S_{ws} C_T^2 \frac{1}{\tau}} \quad (1)$$

where  $A_1$  is a constant depending on the type of the signal shaping [15]. The pulse shaper adjusts the frequency response of the signal and noise to increase the signal to noise ratio since the frequency spectra of the signal and the noise sources all differ [16]. Depending on the noise source, a different shape factor is used.  $A_1$  is a shape factor of the filter for the noise with white spectral density at the input of the amplifier.  $C_T$  is the total capacitance at the preamplifier input. This includes the detector capacitance,  $C_d$ , the feedback capacitance,  $C_f$ , the test capacitance,  $C_t$ , the stray capacitance,  $C_s$  and the input transistor capacitance,  $C_i$ . The latter, also referred as intrinsic gate capacitance, consists of the gate to source capacitance,  $C_{gs}$  and the drain to gate capacitance,  $C_{dg}$ , and they are both voltage dependent capacitances. They arise due to the depletion layer of the junctions which acts as a dielectric and therefore they depends on the source to gate voltage,  $V_{GS}$ , and the drain to gate voltage,  $V_{GD}$ . In most amplifier applications, the drain to gate voltage is greater than the source to gate voltage. The capacitance of an abrupt junction is an inverse function of the square root of the junction voltage [17]. Thus,  $C_{gs}$  is higher than  $C_{dg}$ , this difference becomes even larger when the source to gate junction is forward biased because its depletion layer decreases.

The time parameter,  $\tau$ , is the shaping time of the filter (shaping amplifier). This time parameter is proportional to the width of the  $\delta$ -response of the filter,  $h(t)$  [15]. Since the series white noise is a continuous signal in frequency domain, its spectrum is referred to as power spectral density [18]. A power spectral density has unit of  $V^2 \text{ Hz}^{-1}$  and an important characteristic is that its integral over all possible frequencies equals the average signal power [19]. The series white noise power spectral density,  $S_{ws}$ , (also known as spectral voltage noise density of thermal noise) can be approximated to the thermal noise of a noise resistance,  $R_s$ , in series with the gate [20] such that

$$S_{ws} = 4kTR_s = 4kT \frac{\gamma}{g_m} \quad (2)$$

where  $g_m$  is the FET transconductance which determines the change in drain current,  $I_D$ , due to a change in gate to source voltage,  $V_{GS}$  [21], where

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \quad (3)$$

The parameter  $\gamma$  is the dimensionless product of noise resistance,  $R_s$ , and transconductance,  $g_m$  [22]. The noise resistance,  $R_s$ , is a function of the drain to source voltage,  $V_{GS}$ , and the velocity saturation parameter,  $\gamma'$ . The velocity saturation parameter is a constant dependant on the FET bias condition and the channel length  $l$ . Specifically,  $\gamma'$  is given by

$$\gamma' = \frac{V_p}{lE_0} \quad (4)$$

where  $V_p$  is the pinch-off voltage.  $V_p$  is the corresponding voltage value of drain to source voltage,  $V_{DS}$ , plus the built in voltage  $V_{bi}$

(described in Section 4) where the channel is fully depleted and saturation current flows through the channel, with the gate shorted. Its value depends on the doping density,  $N_D$ , and the geometry of the device, such that

$$V_p = \frac{qh^2 N_D}{2\epsilon\epsilon_0} \quad (5)$$

where  $h$  is the height of the channel (i.e. half the distance between the p-type materials that are connected to the gate terminals in an n channel JFET),  $N_D$  is the doping concentration in the channel and  $\epsilon$  and  $\epsilon_0$  are the relative permittivity of the material and the permittivity of free space, respectively [23]. The parameter  $E_0$  in Eq. (4) is an empirically determined constant which relates the experimental measurements of the carrier mobility,  $\mu$ , in a uniform channel FET with the electric field,  $E$ . For example, the parameter  $E_0$  has been found to be equal to  $0.85 \times 10^4 \text{ V/cm}$  for a n-type silicon material [24]. Hence,  $\gamma'$  is also determined by the material. As an example, for the n-type Silicon JFET, 2N4338, with  $l = 12 \mu\text{m}$  and  $V_p = 1 \text{ V}$ , the velocity saturation parameter  $\gamma'$  equals to 0.098 [11]. From Ref. [22], the parameter  $\gamma$  may be approximated to

$$\gamma = 0.7 + \frac{V_p - V_{GS}}{2lE_0} \quad (6)$$

Alternatively, substituting  $lE_0$  of Eq. (6) with its equal from Eq. (4), and rearranging, the dimensionless product of noise resistance,  $R_s$ , and transconductance,  $g_m$ , produces

$$\gamma = 0.7 + \frac{\gamma'}{2} \left( 1 - \frac{V_{GS}}{V_p} \right) \quad (7)$$

The series white noise dominates at short shaping time due to its inversely proportional relationship with the shaping times (Eq. (1)).

### 2.2. Parallel white noise

Parallel white noise (current noise) arises from the shot noise of the FET gate current,  $I_G$ , and detector's leakage current,  $I_{LD}$  [4]. This is due to the discrete nature of electric charge [25]. Another source of the parallel white noise is the feedback resistor  $R_f$ , in preamplifiers that have them.

From Ref. [4], the ENC of the white parallel noise is given by

$$ENC_{wp} = \frac{1}{q} \sqrt{\frac{A_3}{2} S_{wp} \tau} \quad (8)$$

where  $A_3$  is a constant depending on the shape of the pulse determined by the shaper [15]. This number is the shape factor of the filter for the noise with  $1/f^2$  power spectral density at the input of the shaping amplifier. The parallel white noise power spectral density  $S_{wp}$  (also known as spectral current noise density of shot noise) is

$$S_{wp} = 2q\alpha'(I_{LD} + I_G) + \frac{4kT}{R_f} \quad (9)$$

in which  $\alpha' = 1$  for full shot noise [4]. Full shot noise is present when the motion of electrons can be regarded randomly and independently of each other and hence Poissonian statistics describe the transfer of electrons. Parallel white noise dominates at long shaping times, whereas it can be considered less important than other types of noises at short shaping times (Eq. (8)).

### 2.3. $1/f$ series noise

The  $1/f$  series noise arises from the flicker noise of the drain current of the preamplifier input transistor. This is due to the generation and recombination of carriers in the two depleted

regions from impurity atoms and lattice defects. The fluctuation in the depleted regions' charge changes the width of the channel which results in fluctuations of the drain current,  $I_D$  [25]. If the trapping and releasing of carriers were purely random, the noise spectrum would be uniform. Since this process occurs independently in time, the noise spectrum deviates from white noise, in a certain frequency range [16]. In the rare situation where only one time constant is involved in these events, the power spectral density has a  $1/f^2$  distribution and when more than one time constants are involved, the distribution of the power spectral density becomes a nearly ideal  $1/f$  response.

The ENC of the  $1/f$  series noise is given by Ref. [4] as

$$ENC_{1/f} = \frac{1}{q} \sqrt{A_2 \pi A_f C_T^2} \quad (10)$$

where  $A_2$  is a constant depending on the type of signal shaping [15]. The corresponding spectral voltage noise density is  $A_f/f$ , where  $A_f$  is a constant characteristic of the transistor and can be expressed as

$$A_f = \frac{H_f}{C_i} = \frac{(\gamma 2kT/\pi)(f_c/f_T)}{C_i} \quad (11)$$

where  $f_T$  is the transition frequency and  $f_c$  is the corner frequency of the JFET. The transition frequency,  $f_T$ , is the frequency where the unity current gain is achieved, i.e.  $i_0 = i_i$  [11],

$$f_T = \frac{g_m}{2\pi C_i} \quad (12)$$

The corner frequency,  $f_c$ , is where the white spectral density and the  $1/f$  spectral density are equal. The ratio  $f_c/f_T$  depends only on the bias of the transistor, as can be seen in Section 3.2, Eq. (24). For a given technology and fixed bias conditions,  $H_f$  is constant for FETs that differ only in channel width  $W$  [4].  $1/f$  noise is  $\tau$  independent (Eq. (10)).

#### 2.4. Dielectric noise

Dielectric noise arises from thermal fluctuations in insulators that are close to, or in contact with, the preamplifier input [4]. Polarization in lossy dielectrics can cause fluctuations in electric charge density. The field that is consequently set up, draws current from the external circuit [26]. This current can add substantially to the noise. In other words, the dielectric material is inserted into a stray capacitance and its distribution in the vicinity of the FET gate affects the dielectric noise. The feedback capacitance, test capacitance, the dielectrics of the transistor as well as the material of the PCB all contribute to the dielectric noise. Hence, great attention should be given to their dissipation factors. Also, FET's package and the passivation of its surface may be regarded as lossy dielectrics, which in turn increase the noise of the system.

The ENC for the dielectric noise is given by

$$ENC_D = \frac{1}{q} \sqrt{A_2 2kTDC_{die}} \quad (13)$$

where  $C_{die}$  represents the lossy dielectrics with a (dimensionless) dissipation factor of  $D$ . The dissipation factor  $D$  is defined as

$$D = \frac{G(\omega')}{\omega' C_{die}} \quad (14)$$

where  $G(\omega')$  is the loss conductance at an angular frequency  $\omega'$  associated with the lossy capacitance  $C_{die}$  [26]. Each capacitance in the system can be regarded as lossy, with an associated dissipation factor and is considered separately. The dissipation factor for low loss dielectrics is in the range of  $10^{-5}$  [26], whereas lossy materials exhibit higher  $D$  resulting in higher dielectric noise. For example, the dissipation factor for Si is  $2 \times 10^{-4}$  [26].

Lossy dielectrics generate a noise current spectrum in parallel with the input, proportional to  $f$ , which when integrated on the input capacitance becomes  $1/f$  noise [20]. The dielectric noise contribution is independent of both the input capacitance and the shaping time constant  $\tau$  (Eq. (13)). Eliminating the package of the FET by integrating the FET's die onto the detector is clearly advantageous [7] as is integrating the FET with the detector as in a DEPFET detector [27].

#### 2.5. Induced gate current noise

Induced gate current noise arises from fluctuations in the gate charge due to fluctuations in the drain current [25]. This is caused from the capacitive coupling between the gate and the channel of the JFET. Since both stem from the same noise origin, the random motion of carriers in the channel, the induced gate current noise,  $S_{ig}$ , is correlated with the drain current noise,  $S_{ws}$ , with an imaginary coefficient  $c = j c_0$  [4].

The power spectral density of the induced gate current noise is proportional to frequency,  $\omega$ , and is given by

$$S_{ig} = S_{ws} \omega^2 C_{gs}^2 \delta \quad (15)$$

where both  $\delta$  and  $c_0$  are experimentally measured factors [4]. The factor  $\delta$ , which is dimensionless and depends upon the bias condition, was calculated for a simplified FET model by Bertuccio et al. [4] to be  $\delta \approx 0.25$ .

The correlation factor,  $c_0$ , between the drain current,  $I_D$ , and the induced gate charge is a function of the pinch-off voltage,  $V_p$ , the voltage at the gate,  $V_{GS}$ , the voltage at the drain,  $V_{DS}$ , and the diffusion potential of the gate-channel junction,  $V_{dif}$  (also known as built-in voltage [28]) [29]. By definition, it can be calculated once the gate current noise,  $S_{ig}$ , and the drain current noise,  $S_{ws}$ , are calculated. In saturation,  $c_0$  has been previously calculated using an approximation method which allowed the calculation of  $S_{ig}$  and  $S_{ws}$ , resulting in a value of  $c_0$  to be approximately 0.4 [29]. The corresponding equivalent noise charge,  $ENC_{wsc}$ , which takes into account  $S_{ws}$ ,  $S_{ig}$  and their correlation [4] equals

$$ENC_{wsc} = \frac{1}{q} \sqrt{A_1 S_{ws} G_c C_T^2 \frac{1}{\tau}} = ENC_{ws} \sqrt{G_c} \quad (16)$$

where,

$$G_c = \left[ 1 + \left( \frac{C_{gs} \delta}{C'_d + C_i} \right)^2 - \frac{2c_0 C_{gs} \delta}{C'_d + C_i} \right] \quad (17)$$

$G_c$  is a correction factor which enhances or reduces the contribution of the white series noise (Eq. (16)).

The induced gate current noise can be important at short shaping times where the white series noise can be dominant.

### 3. Contribution of the input JFET

The contribution of the input transistor to the total noise of the system is examined in this section. Although in traditional cooled Si FETs the total noise is often dominated by the  $1/f$  and the white series noise [30], in wide bandgap spectroscopy systems operating at high temperatures, the parallel white noise and the dielectric noise can be of great significance [31,32]. The input transistor's contribution is examined by expressing the total squared equivalent noise charge of the system in terms of the detector's and transistor's parameters while the detector is assumed to be ideal (i.e. no noise arises from it) in Section 3.2. Thereinafter, the capacitance matching of the input transistor to the detector is presented in Section 3.3. Lastly, the gate current of the JFET is explained in Section 3.4.

### 3.1. Squared equivalent noise charge

The squared equivalent noise charge [10] is useful for computing the total ENC from all noise sources, such that

$$\text{ENC}^2 = \frac{1}{q^2} \left( aC_T^2 A_1 \frac{1}{\tau} + bA_3 \tau + 2\pi a_f C_T^2 A_2 + \frac{b_f}{2\pi} A_2 \right) \quad (18)$$

The total squared equivalent noise charge simply originates from summing the ENC from all noise components in quadrature. The first term in Eq. (18) is the series white noise, the second term is the parallel white noise, the third term is the  $1/f$  noise and the fourth term is the dielectric noise (the induced gate current noise has been excluded). The dependency of the  $\text{ENC}^2$  on the shaping time,  $\tau$ , is emphasized in Eq. (18).

In Eq. (18),  $a$  (measured in  $\text{V}^2/\text{Hz}$ ) is the contribution of the white series noise and is given by

$$a = \gamma \frac{2kT}{g_m} \quad (19)$$

This is derived by comparing Eq. (18) with Eqs. (1) and (2).

In Eq. (18),  $b$  (measured in  $\text{A}^2/\text{Hz}$ ) is the contribution of the white parallel noise, such that

$$b = q(I_{LD} + I_G) \quad (20a)$$

This is derived by comparing Eq. (18) with Eqs. (8) and (9), for the case that there is no feedback resistor,  $R_f$ . However, when there is feedback resistor  $R_f$ , the contribution of the white parallel noise becomes

$$b = q(I_{LD} + I_G) + \frac{2kT}{R_f} \quad (20b)$$

In Eq. (18),  $a_f$  is the coefficient of the  $1/f$  noise, where

$$a_f = \frac{(\gamma 2kT/\pi)(f_c/f_T)}{2C_i} \quad (21)$$

This is derived by comparing Eq. (18) with Eqs. (10) and (11).

Lastly, in Eq. (18),  $b_f$  is the coefficient for the dielectric noise and equals

$$b_f = 4kT\pi DC_{die} \quad (22)$$

This is derived by comparing Eq. (18) with Eq. (13).

### 3.2. Contribution of the input transistor to the total noise in summary

The overall ENC is calculated using Eq. (18). The intention of this is to elucidate which JFET parameters affect the noise and how they do so. The first approximation to the problem is by assuming that the detector capacitance,  $C_d$ , is negligible and only the transistor's input capacitance,  $C_i$ , is regarded as the total capacitance,  $C_T$ . Also, the detector's leakage current,  $I_{LD}$ , is assumed to be zero. Making all other sources of noise ideal, the ENC which arises only from the input JFET is computed. Hence, Eq. (18) becomes

$$\text{ENC}^2 = \frac{1}{q^2} \left( \gamma \frac{2kT}{g_m} C_i^2 A_1 \frac{1}{\tau} + qI_G A_3 \tau + (\gamma 2kT) \left( \frac{f_c}{f_T} \right) C_i A_2 + 2kTDC_i A_2 \right) \quad (23)$$

The parameters of the input FET that *directly* affect the ENC are its gate current,  $I_G$ , its input capacitance,  $C_i$ , the ratio between the corner and transition frequency,  $f_c/f_T$ , its transconductance,  $g_m$ , and the dissipation factor,  $D$ , of the JFET's material.

The ENC contribution of some different FETs due to the white parallel noise was plotted by Bertuccio et al. using Eq. (8). (Fig. 1 in Ref. [4]); the equivalent noise charge was plotted as a function of FETs' gate leakage current (which is part of gate current  $I_G$  as is explained in Section 3.4) with  $\tau$  as a parameter. The transistor's gate leakage current is a source of parallel white noise and should

be minimized. It can be clearly seen from Fig. 1 in Ref. [4] that it is the dominant source of noise at long shaping times and can be negligible at short  $\tau$ .

The ENC contribution of different FETs due to the series white noise was plotted by Bertuccio et al. using Eq. (1) (Fig. 2 in Ref. [4]). The equivalent noise charge was plotted as a function of  $K_s$  with  $\tau$  as a parameter, where, was used for comparison purposes [4]. Increases in the transistor's gate intrinsic capacitance,  $C_i$ , (included in the total capacitance,  $C_T$ ) cause larger drain current shot noise contributions at the output and hence  $C_i$  should be kept as low as possible to limit the series white noise. It can be clearly seen from Fig. 2 in Ref. [4] that  $C_i$  is a significant source of noise at short shaping times and can be negligible at long shaping times.

Regarding the ratio  $f_c/f_T$ , it can be seen from Eq. (23) that it should be minimized for the  $1/f$  noise to be minimized. This ratio is given by the following equation [11],

$$\frac{f_c}{f_T} = \frac{q|V_{GS} - V_p|\alpha_{1/f}}{kT} \quad (24)$$

in which  $V_{GS}$  is the gate to source voltage, and  $\alpha_{1/f}$  is a dimensionless  $1/f$  parameter (also known as the Hooge parameter) which depends on the quality of the semiconductor material and any damage present in the FET. For instance, this parameter depends on whether or not the current in the JFET flows through a region damaged by implantation [11]. Hence, this parameter cannot be directly analytically calculated in theory, but it can be calculated, once  $f_c$  is experimentally observed, using the equation,

$$\alpha_{1/f} = \frac{f_c 2\pi kT C_i}{q g_m |V_{GS} - V_p|} \quad (25)$$

The corner frequency,  $f_c$ , can be obtained by measuring the equivalent input spectral voltage noise density squared (in  $\text{V}^2/\text{Hz}$ ) of the JFET. This noise includes both the white series noise (Section 2.1) and the  $1/f$  noise (Section 2.3). The  $1/f$  parameter,  $\alpha_{1/f}$ , should be as small as possible to minimise the ratio  $f_c/f_T$ , as can be seen from Eq. (24). This consequently results in requiring the transistor input capacitance,  $C_i$ , to be as low as possible and the transistor transconductance,  $g_m$ , to be as high as possible. This is in agreement with Eq. (23), where, by having a large a value of transconductance, the series white noise spectral density is decreased and the overall ENC is also decreased.

Two other transistor parameters which indirectly affect the noise are the gate length,  $l$ , and the channel width,  $W$ . Both the transconductance and the transistor input capacitance are proportional to the channel width such that

$$g_m = \frac{Whq\mu N_D}{l} \left( 1 - \sqrt{\frac{-V_{GS} + V_{bi}}{V_p}} \right) \quad (26)$$

where  $\mu$  is the carrier mobility,  $V_{bi}$  and  $V_p$  are the built in voltage and the pinch off voltage respectively; both are defined in Section 4. The capacitance for a one-sided abrupt junction, as the gate to channel junction can be regarded, is given by

$$C_i = \frac{\epsilon \epsilon_0 W l}{H(x)} \quad (27)$$

where  $H(x)$  is the width of the depletion region at a distance  $x$  from the source and is function of  $V_{GS}$  [23].

Since the goal is to have transistor input capacitance,  $C_i$ , as small as possible and the transconductance,  $g_m$ , as high as possible, as has been made clear above, there is a trade off in selecting the ideal channel width.

When the detector capacitance dominates ( $C_d \gg C_i$ ), increasing the channel width results in only negligible increment of transistor input capacitance, where at the same time the increased transconductance leads to lower ENC [16]. When the transistor



input capacitance dominates ( $C_d < C_i$ ) and the width of the channel is increased, the positive contribution of the higher transconductance to the total noise is overridden by the increased transistor input capacitance,  $C_i$ . It should be noted here that in the capacitively matched case ( $C_d = C_i$ ), the total ENC is minimized (see Section 3.3).

Since the transistor input capacitance,  $C_i$ , is proportional to the gate length (Eq. (27)), it is decreased as  $l$  is decreased resulting in higher transition frequency,  $f_T$  (Eq. (12)). Furthermore, a smaller gate length,  $l$ , results in a higher transconductance (Eq. (26)). Hence, decreasing the channel length has a positive effect at both the series white noise and  $1/f$  noise. However, the smaller the gate length,  $l$ , the higher the drain current,  $I_D$ , becomes [28], i.e.

$$I_D \propto \frac{1}{l} \quad (28)$$

Since part of the gate to channel leakage current (which is part of  $I_G$  as explained in Section 3.4) is a linear function of drain current,  $I_D$ , it increases with decreased gate length,  $l$ , [33] (the total  $I_G$  is analyzed in Section 3.4). This results in increased parallel white noise.

Moreover, the transition frequency,  $f_T$ , in the non-saturated case,  $f_{Tns}$ , is given by Ref. [23] as

$$f_{Tns} = \frac{\mu V_{DS}}{2\pi l^2} \quad (29a)$$

and in the saturation case as

$$f_{Ts} = \frac{v_s}{2\pi l} \quad (29b)$$

where  $\mu$  is the carrier mobility (electron mobility in an n-channel and hole mobility in a p-channel JFET [28]). The non-saturated case refers to relatively low internal (to the device) electric field,  $E$ , where the proportionality of the carrier velocity,  $v_d$ , to the magnitude of the electric field still holds [28]. For higher electric fields, the carrier velocity equals the saturation velocity,  $v_s$ , and does not further increase with electric field increment. The trade off in selecting the gate length,  $l$ , has been already discussed. Maintaining a high transition frequency requires high carrier mobility in the channel (Eq. (29a)). However, for short channel length JFETs, the carrier velocity saturates at low drain to source voltages,  $V_{DS}$ , and the transition frequency becomes proportional to the saturation velocity (Eq. (29b)). Hence, materials with higher carrier saturation velocity are advantageous.

### 3.3. Matching detector and transistor capacitance

The requirements for transistor's parameters when  $C_d = 0$  were discussed in Section 3.2. However, in this section, the detector capacitance,  $C_d$ , is not assumed to be zero. Hence,

$$C_T = C_d + C_f + C_t + C_s + C_i = C'_d + C_i \quad (30)$$

where  $C'_d$  is the input load capacitance and all the other capacitances have been defined in Section 2.1.

Starting from Eq. (1), it can be shown that transistor input capacitance  $C_i$ , should match the input load capacitance  $C'_d$ . Substituting the series white noise spectral density (Eq. (2)) into Eq. (1),  $ENC_{ws}$  is shown to be

$$ENC_{ws} = \frac{1}{q} \sqrt{\frac{A_1 \gamma}{2\tau} \frac{4kT}{g_m} C_T^2 \frac{1}{\tau}} \quad (31.1)$$

Substituting the transconductance from Eq. (12) into the above Eq. (31.1) and rearranging

$$ENC_{ws} = \frac{1}{q} \sqrt{\frac{A_1 \gamma}{2\tau} \frac{4kT}{f_T 2\pi} \frac{C_T}{\sqrt{C_i}}} \quad (31.2)$$

Substituting  $C_T$  from Eq. (30) into Eq. (31.2):

$$ENC_{ws} = \frac{1}{q} \sqrt{\frac{A_1 \gamma}{2\tau} \frac{4kT}{f_T 2\pi} \frac{C'_d + C_i}{\sqrt{C_i}}} \quad (31.3)$$

Taking the square root and squaring  $C'_d$  and  $C_i$ , and rearranging,  $ENC_{ws}$  equals:

$$ENC_{ws} = \frac{1}{q} \sqrt{\frac{A_1 \gamma}{2\tau} \frac{4kT}{f_T 2\pi}} \left( \sqrt{C'_d} \sqrt{\frac{C'_d}{C_i}} + \sqrt{C_i} \sqrt{\frac{C_i}{C_i}} \right) \quad (31.4)$$

where the fraction  $C_i/C_i (=1)$  is substituted with the fraction  $C'_d/C'_d (=1)$

$$ENC_{ws} = \frac{1}{q} \sqrt{\frac{A_1 \gamma}{2\tau} \frac{4kT}{f_T 2\pi}} \sqrt{C'_d} \left( \sqrt{\frac{C'_d}{C_i}} + \sqrt{\frac{C_i}{C'_d}} \right) \quad (31.5)$$

where the fraction  $C'_d/C_i$  is substituted with the parameter  $m$

$$ENC_{ws} = \frac{1}{q} \sqrt{\frac{A_1 \gamma}{2\tau} \frac{4kT}{f_T 2\pi}} \sqrt{C'_d} (m^{1/2} + m^{-1/2}) \quad (32)$$

Substituting  $A_f$  (Eq. (11)) into Eq. (10) and rearranging as above, gives

$$ENC_{1/f} = \frac{1}{q} \sqrt{A_2 \gamma 2kT \frac{f_c}{f_T} C'_d} (m^{1/2} + m^{-1/2}) \quad (33)$$

In order to minimise the white series noise and the  $1/f$  noise, low capacitance detectors,  $C_d$ , transistors with the highest  $f_T$  (Eq. (12)) and highest ratio  $f_T/f_c$  (Eq. (24)) are required. Regarding the ideal transistor, high  $f_T$  is achieved with high transconductance,  $g_m$ , and low input capacitance,  $C_i$ , as seen from Eq. (12).

However, it can be seen from Eqs. (32) and (33), that low white series and  $1/f$  noise requires capacitively matching the transistor with the input load capacitance,  $C'_d$ . Consequently, the ideal transistor has an input capacitance  $C_i$  which depends on the detector and all other input capacitances.

Hence, when

$$C_i = C'_d = C_d + C_f + C_t + C_s \quad (34)$$

$m=1$ , and consequently lower white series and  $1/f$  noises are achieved. Overall, the aim is to decrease  $C'_d$  as much as possible and then match the transistor input capacitance  $C_i$  to that value.

### 3.4. Gate current

The characteristics of the ideal input FET, in terms of noise, have been discussed in the previous sections. However, the requirements for the input JFET are also affected by the specific application. In preamplifier circuits where an n-channel JFET is used in the forward bias mode (a p-channel JFET can also be employed in the forward bias mode) there is no feedback resistor [6] and consequently the parallel white noise is reduced. However, the operating bias point ( $V_{GS}$ ) in this specific configuration sets the gate current,  $I_G$ , the transconductance,  $g_m$ , and the transistor input capacitance,  $C_i$ .

In the conventional (i.e. reverse bias) mode of a JFET, ideally, the current flowing at the gate,  $I_{GRM}$ , is zero. However, in a real transistor, there are three components which constitute the gate current [17]. Two of them are the leakage current flowing at the gate to drain junction,  $I_{DGI}$ , and the leakage current flowing at the gate to source junction,  $I_{GSI}$ , whose directions depend on whether the JFET is n- or p-channels. They simply result from two processes: *thermal ionization* (generation) of carriers within the depletion regions of the junctions and *diffusion of minority carriers* due to reverse biasing. The third component,  $I_3$ , results from carriers generated in the drain to gate depletion region from

impact ionization by the drain current carriers. This current,  $I_3$ , is linear function of  $I_D$  and exponential function of  $V_{DG}$  [17]. The summation of the drain to gate leakage current  $I_{DGL}$  and  $I_3$  is termed the total drain to gate current,  $I_{DG}$ .

$$I_{DG} = I_{DGL} + I_3 \quad (35)$$

and the total gate current,  $I_{GRM}$ , when the JFET operates in the reverse (conventional) mode is given by

$$I_{GRM} = I_{GSI} + I_{DG} \quad (36)$$

When the JFET is used in forward bias mode (i.e. with the gate slightly positive), the gate to source junction conducts like a normal diode, and  $I_{GS}$  is formed from majority carriers (rather than being the leakage current  $I_{GSI}$  resulting from the diffusion of minority carriers). The drain to source junction is still reverse biased, and leakage current,  $I_{DGL}$ , flows. The third component,  $I_3$ , is still present. The gate current,  $I_{GFM}$ , consists of the summation of these three components, and all of them contribute to the parallel white noise (Eq. (9)).

In this mode, the input FET is forward biased by the leakage current of the detector,  $I_{LD}$ , which enters the preamplifier at the gate of the FET and also the current from drain to gate  $I_{DG}$ . Both currents flow from gate to source junction. Hence,  $I_{GS}$  equals to:

$$I_{GS} = I_{LD} + I_{DG} \quad (37)$$

and the total gate current when the JFET is used in the forward bias mode,  $I_{GFM}$ , is

$$I_{GFM} = I_{GS} + I_{DG} = I_{GS} + I_{DGL} + I_3 \quad (38)$$

Combining Eqs. (37) and (38),  $I_{GFM}$  can be obtained

$$I_{GFM} = I_{LD} + 2I_{DG} \quad (39)$$

A reduction of the total noise of the system is achieved by minimizing all three components of Eq. (38). The gate to source,  $I_{GS}$ , current is minimized by using a detector with low leakage current; at high temperatures this can require a detector made from a wide bandgap material such as SiC [34] or AlGaAs [35]. The drain to gate leakage current,  $I_{DGL}$ , can be kept to a minimum by keeping the junction at low temperature but unfortunately this is not always a practical option; as a consequence, wide bandgap FETs (Section 4) are required for high temperature environments; as an approximation in Si, thermal ionization of carriers double in magnitude for each 10 °C temperature increase [17]. The third component,  $I_3$ , is decreased as the drain current,  $I_D$ , decreases. Since the input JFET is used in the saturation region, and the drain current in saturation is proportional to drain to source saturation current with gate shorted,  $I_{DSS}$ , a JFET with relatively small  $I_{DSS}$  should be used [28].

For simplicity reasons, and since  $I_{GS}$  is bigger than  $I_{DG}$ , in the forward bias mode, the gate to source current,  $I_{GS}$ , is sometimes referred as the gate current  $I_{GFM}$ , and Eq. (38) takes the following form

$$I_{GFM} \approx I_{GS} = I_{LD} + I_{DG} \approx I_{LD} \quad (40)$$

The contributions of these two components to the parallel white noise (Eq. (9)),  $I_{LD}$  and  $I_{GFM}$ , are regarded separately due to there being two statistically independent shot noises which arise from them (i.e. shot noise of  $I_{LD}$  and shot noise of  $I_{GFM}$ ). Detector leakage current,  $I_{LD}$ , can vary from less than 1 pA [12] to hundreds of pA, or even nA, depending on detector type and temperature.

#### 4. Wide bandgap materials

In this section, the advantages of a wide bandgap JFET, such as SiC, over Si are examined. This is done by comparing the noise contribution of two identical JFETs with their only difference being

the semiconductor material. More specifically, the noise arising from a previously reported n-channel 6H-SiC JFET is computed at different shaping times and room temperature when operating under normal conditions in a charge sensitive preamplifier without the feedback resistor ( $V_{DS}$  in the saturation region and  $V_{GS} > 0$ ). Thereinafter, the noise arising from the same geometry JFET made of Si is calculated and compared to the former case.

An epitaxial n-channel 6H-SiC JFET is used [36]. Its channel length, width and height are  $l = 10 \mu\text{m}$ ,  $w = 100 \mu\text{m}$ , and  $h = 0.3 \mu\text{m}$  respectively; the donor concentration in the channel,  $N_D$ , and the acceptor concentration in the gate,  $N_A$ , are  $1 \times 10^{23} \text{ m}^{-3}$  and  $2 \times 10^{25} \text{ m}^{-3}$ , respectively [36].

##### 4.1. Model calculations

The noise contribution was computed using Eq. (23). The input capacitance,  $C_i$ , was calculated using Eq. (27) and it was assumed that only the gate to source junction contributes to its input capacitance (see Section 2.1). Hence,

$$C_i \approx \frac{\epsilon \epsilon_0 W (\frac{l}{2})}{W_s} \quad (41)$$

where  $W_s$  (the gate to source depletion region width) is calculated, in accordance with Ref. [23], by

$$W_s = \sqrt{\frac{2\epsilon \epsilon_0}{qN_D} (-V_{GS} + V_{bi})} \quad (42)$$

The built in potential between the p-n junction,  $V_{bi}$ , equals

$$V_{bi} = \frac{kT}{q} \ln \frac{N_D N_A}{n_i^2} \quad (43)$$

in which  $N_A$  is the doping concentration of the p-type gate (in an n-channel JFET) and  $n_i$  is the intrinsic carrier concentration given by

$$n_i = \sqrt{N_c N_v} e^{-E_g/2kT} \quad (44)$$

$E_g$  is the bandgap of the semiconductor material and  $N_c$  and  $N_v$  are the effective density of states in the conduction and valence bands respectively [23].

The transconductance,  $g_m$ , was calculated using Eq. (26). The ratio  $f_c/f_T$  was calculated using Eq. (24).

The dimensional  $1/f$  parameter,  $a_{1/f}$ , depends on the quality of the JFET material and material damage [11], as has been discussed in Section 3.2. The  $a_{1/f}$  values often observed after 1980 for Si JFETs are  $10^{-8} < a_{1/f} < 10^{-6}$  [11]. For SiC JFETs, this value has typically been measured to be higher, reaching a value of  $a_{1/f} \approx 10^{-6}$  after proper annealing [37,38]. Since this dimensionless parameter cannot be analytically calculated based on the geometry and the material of each device, for the current modeling moderate values of  $10^{-7}$  and  $10^{-6}$  have been used for the Si and SiC JFETs, respectively.

The gate current was computed from Eq. (39) taking into account only the contribution of the input JFET ( $I_{LD} = 0$ ) such that

$$I_{GFM} = 2I_{DG} = 2(I_{DGL} + I_3) \quad (45)$$

where the leakage current at the drain to gate junction was computed by

$$I_{DGL} = A_{DG} \left( \frac{qD_p n_i^2}{L_p N_D} + \frac{qD_n n_i^2}{L_n N_A} + \frac{qn_i W_D}{\tau_g} \right) \quad (46)$$

where  $A_{DG}$  is the cross section area of the junction [39]. The sum of the first two terms in Eq. (46) is the saturation current due to diffusion,  $I_{diff}$ , (holes diffuse to n-type and electrons to p-type), and the third term is the generation current due to reduction in carrier concentration under reverse bias,  $I_{gen}$  [39]. The hole diffusion coefficient,  $D_p$ , and the electron diffusion coefficient,  $D_n$ , were

computed from the Einstein relation

$$D_p = \frac{kT}{q} \mu_h \quad (47a)$$

$$D_n = \frac{kT}{q} \mu_e \quad (47b)$$

where  $\mu_h$  and  $\mu_e$  are the hole and electron mobility in the semiconductor material. The hole diffusion length  $L_p$  and the electron diffusion length  $L_n$  were computed by

$$L_p = \sqrt{D_p \tau_p} \quad (48a)$$

$$L_n = \sqrt{D_n \tau_n} \quad (48b)$$

where  $\tau_p$  and  $\tau_n$  are the hole and electron lifetime respectively [23]. The generation current takes place in the depletion region between the drain and gate, which has a depletion-layer width,

$$W_D = \sqrt{\frac{2\epsilon\epsilon_0}{qN_D}(V_{DG} + V_{bi})} \quad (49)$$

The generation carrier lifetime  $\tau_g$  in Eq. (46) was calculated by

$$\tau_g = \left(1 + \frac{n}{n_i}\right) \tau_p + \left(1 + \frac{p}{n_i}\right) \tau_n \quad (50)$$

where  $p$  and  $n$  are the hole and electron concentrations in the depletion region and are both functions of the applied voltage and the distance from the two boundaries of the depletion region and the n and p sides [39]. For a given applied voltage,  $V_{DG}$ , the electron concentration,  $n$ , starts from a maximum value of  $n_n$  ( $=N_D$ ) at the boundary of the depletion region with the n side and decreases to a minimum value of  $n_p$  at the boundary of the depletion region with the p type side, where, in accordance with Ref. [23],

$$n_p = \frac{n_i^2}{N_A} \exp\left(\frac{qV_{DG}}{kT}\right) \quad (51)$$

Similarly, for a given applied voltage,  $V_{DG}$ , the hole concentration,  $p$ , starts from a maximum value of  $p_p$  ( $=N_A$ ) at the boundary of the depletion region with the p side and decreases to a minimum value of  $p_n$  at the boundary of the depletion region with the n type side, where, as per Ref. [23],

$$p_n = \frac{n_i^2}{N_D} \exp\left(\frac{qV_{DG}}{kT}\right) \quad (52)$$

Since the product  $np$  of the electron and hole concentration is constant for a given applied voltage at both the boundaries of the depletion region as well as at all the intermediate points, the electron and hole concentration at the boundary of the depletion

region with the n side was used to calculate the generation lifetime,  $\tau_g$  (Eq. (50)).

The impact ionization current,  $I_3$ , is normally negligible at low  $V_{DG}$ , where the leakage current of the junction is dominant [17]. Moreover,  $I_3$  decreases with increasing temperature due to its dependant on carrier mobility. For simplicity reasons, the impact ionization current  $I_3$  is considered negligible in the present calculations. However, its linear function with the drain current  $I_D$  implies that JFETs with lower  $I_D$  are favorable. The drain current at saturation region  $I_{Dsat}$  was computed by

$$I_{Dsat} = \frac{W\mu q^2 h^3}{6\epsilon\epsilon_0 l} N_{Deff} n_{ch} \left[ 1 - 3 \left( \frac{-V_{GS} + V_{bi}}{V_p} \right) + 2 \left( \frac{-V_{GS} + V_{bi}}{V_p} \right)^{3/2} \right] \quad (53)$$

where the effective donor concentration  $N_{Deff}$  at the channel is approximately equal to  $N_D$ , and  $n_{ch}$  is the electron concentration at the channel region which equals to  $N_D$  for Si at room temperature (where the carrier concentration is fully activated). The ionized carrier concentration in the channel,  $n_{ch}$ , is much lower than  $N_D$ , for the SiC JFET, at room temperature (not all carriers are activated) and it was computed to be  $9 \times 10^{21} \text{ m}^{-3}$  based on experimental results according to Ref. [36].

#### 4.2. Material properties

The values of the materials' properties used for the present modeling can be seen at Table 1. It should be noted that the parameters given are temperature,  $T$ , and dopant concentration dependent. Consequently, the used values should be changed for conditions other than those stated.

#### 4.3. Computed parameters

In this paragraph, the computed JFET's parameters using the equations described in Section 4.1 are presented and discussed. For equality of comparison, both JFETs are assumed to have the same geometry and doping concentrations. All calculations are done for  $T=300 \text{ K}$ ,  $V_{GS}=0.2 \text{ V}$  (slightly positive gate as required in a feedback resistorless preamplifier [6]) and  $V_{DS}=9 \text{ V}$  (JFET operating in saturation region i.e.  $V_{DS} \geq V_T$  and thus  $I_D = I_{Dsat}$ ) unless otherwise specified. A comparison between the computed parameters for the two JFETs is presented in Table 2.

Due to its wider bandgap, SiC has much lower intrinsic carrier concentration  $n_i$  (Eq. (44)) compared to Si at a given temperature (here  $T=300 \text{ K}$ ). In other words, fewer carriers are thermally generated in SiC than in Si. This has a number of effects.

First of all, smaller  $n_i$  results in higher built in voltage  $V_{bi}$  (Eq. (43)) which in turns results in lower input capacitance,  $C_i$  (Eq.

**Table 1**

Values of properties used in this study for Si and 6H-SiC for  $T=300 \text{ K}$ ,  $N_D=1 \times 10^{23}$  and  $N_A=2.2 \times 10^{24}$ . With the exception of the dissipation factors for Si [26] and SiC [40], the physical properties for both materials were drawn from Ref. [41].

Parameter	Si	6H-SiC
Dielectric constant	11.70	9.66
Bandgap (eV)	1.12	2.96
Effective density of states in the conduction band ( $\text{m}^{-3}$ )	$3.2 \times 10^{25}$	$9.0 \times 10^{24}$
Effective density of states in the valence band ( $\text{m}^{-3}$ )	$1.8 \times 10^{25}$	$2.5 \times 10^{25}$
Electron mobility ( $\text{m}^2 \text{V}^{-1} \text{s}^{-1}$ )	0.1400	0.0400
Hole mobility ( $\text{m}^2 \text{V}^{-1} \text{s}^{-1}$ )	0.0450	0.0090
Electron lifetime (s)	$5 \times 10^{-6}$	$1 \times 10^{-9}$
Hole lifetime (s)	$2 \times 10^{-5}$	$4.5 \times 10^{-7}$
Dissipation factor	$2 \times 10^{-4}$	$\approx 10^{-6}$

**Table 2**  
Comparison between computed parameters for the Si and the SiC devices.

	Si JFET	SiC JFET
Intrinsic carrier concentration ( $\text{m}^{-3}$ )	$8.61 \times 10^{15}$	$1.88 \times 10^0$
Built in voltage (V)	0.978	2.841
Input capacitance (pF)	0.51	0.25
Transconductance (mS)	4.48	0.84
Corner frequency over transition frequency	$2.61 \times 10^{-5}$	$3.18 \times 10^{-4}$
Gate current (pA)	4.22	$8 \times 10^{-30}$
Drain current (mA)	11	0.2

(41)) i.e. the gate to source depletion region is wider in the SiC JFET compared to Si JFET. The biggest effect of the intrinsic carrier concentration is at the gate current (Eq. (46)), as it can be seen in Table 2. The gate current (with the impact ionization current,  $I_3$ , excluded) in the SiC JFET is 30 orders of magnitude lower than the Si JFET at  $T=300$  K. For higher drain to source voltages,  $V_{DS}$ , where the impact ionization component dominates, the difference between the gate current at the Si JFET and the SiC JFET becomes even bigger due to its linear dependency on the drain current  $I_D$  ( $\sim 50$  times higher in the Si JFET than in the SiC JFET). The effect of the gate length,  $l$ , on the equivalent noise charge was discussed in Section 3.2. Although decreasing the gate length results in higher drain current at saturation region  $I_{Dsat}$  (Eq. (53)), which in turn increases the gate current (due to larger  $I_3$ ), this effect is smaller in wide bandgap semiconductor JFETs compared to Si.

As far as the transconductance is concerned, the higher electron mobility in Si has a more positive effect compared to SiC (Eq. (26)). Also, the ratio between the corner and transition frequency,  $f_c/f_T$ , has found to be higher in the SiC JFET than in the Si JFET, resulting in higher  $1/f$  noise. This is due to the different Hooge parameter.

#### 4.4. Equivalent noise charge

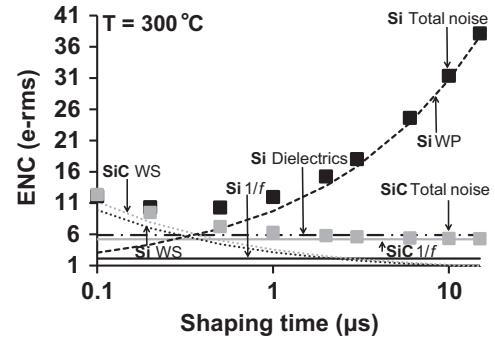
Once the parameters of both JFETs were computed using the equations from Section 4.1, the equivalent noise charge, ENC, arising from the input JFET was calculated using Eq. (23). The calculated overall ENC for both JFETs as a function of the shaping time,  $\tau$ , at  $T=300$  K can be seen in Fig. 1.

For the Si JFET, its sub-microsecond ENC is limited by its white series noise (arising from the ratio  $C_i^2/g_m$ ) and by its dielectric noise. As the shaping time increases ( $\tau > 0.5 \mu\text{s}$ ), the white parallel noise becomes dominant (arising from the gate current), increasing further the equivalent noise charge.

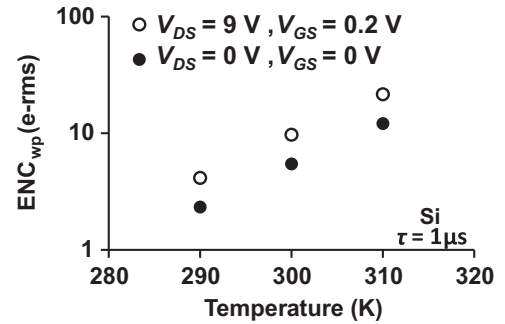
The SiC JFET is also limited by its white series noise in the sub-microsecond shaping time range. Although both transistors have comparable white series noise in this shaping time range, and the  $1/f$  series noise is higher in the SiC JFET than in Si JFET, the overall computed ENC of the SiC device is approximately equal to the Si device. This is due to the lower dissipation factor of the SiC material compared to Si resulting in lower dielectric noise.

In contrast with the Si JFET, as the shaping time becomes longer, the overall ENC for the SiC JFET decreases. At long shaping times the white parallel noise dominates. Since the gate current in the SiC JFET is negligible, a shaping time increase reduces the equivalent noise charge arising from the SiC device, reaching the lower limit set by the  $1/f$  noise, as shown in Fig. 1.

The contribution of the white parallel noise to the overall ENC for the Si JFET is emphasized. The  $\text{ENC}_{wp}$  was computed for the Si device at  $T=300$  K using the parameters stated at Table 1. Although these parameters are temperature dependent, they can be regarded unchanged for small temperature changes. Hence, making the assumption that the parameters of Table 1 are stable for the temperature range  $300 \pm 10$  K, the equivalent noise charge



**Fig. 1.** Calculated equivalent noise charge for a Si JFET (black symbols) and a SiC JFET (gray symbols) at  $T=300$  K having the same geometry (contribution of only the input JFET is included). Total noise – squares; White parallel (WP) noise – square dots; White series (WS) noise – round dots;  $1/f$  noise – solid line; Dielectric noise – long dash dots. The white parallel and dielectrics noise of the SiC JFET are not included in the graph since their contribution is less than  $1 \text{ e}^- \text{ rms}$ .



**Fig. 2.** Calculated equivalent noise charge contribution due to white parallel noise for the Si JFET at  $\tau=1 \mu\text{s}$  under two bias conditions.

contribution due to white parallel noise was calculated at the same temperature range for the Si JFET and  $\tau=1 \mu\text{s}$ . The calculated  $\text{ENC}_{wp}$  for the Si device at different temperatures and bias conditions can be seen in Fig. 2.

At room temperature, the generation current,  $I_{gen}$ , dominates in Si, rather than the diffusion current,  $I_{diff}$  [23]. At a given temperature,  $I_{gen}$  is proportional to the gate to drain depletion layer width,  $W_D$ , (Eq. (46)) which, in turn, is proportional to the square root of the applied voltage,  $V_{DG}$  (Eq. (49)). Hence, it can be further seen that  $\text{ENC}_{wp}$  is highly dependent on  $T$ . For a 10 K temperature rise (from 300 K to 310 K), the equivalent noise charge contribution due to white parallel noise (arising from gate current) increased from  $9 \text{ e}^- \text{ rms}$  to  $21 \text{ e}^- \text{ rms}$ , when  $\tau=1 \mu\text{s}$  and the JFET is under normal operating conditions (i.e. in saturation region with the gate slightly positive). The dependency of the  $\text{ENC}_{wp}$  to  $T$  can be explained as follows: the generation current,  $I_{gen}$ , which dominates at this temperature range, highly depends on the intrinsic carrier concentration  $n_i$  (Eq. (46)). Its temperature dependence is given by

$$I_{gen} \propto n_i \propto \exp\left(-\frac{E_g}{2kT}\right) \quad (54)$$

Including the function of  $\tau_g$  with temperature, the current at the drain to gate junction of the Si JFET used in this study, biased at  $V_{DS}=9 \text{ V}$  and  $V_{GS}=0.2 \text{ V}$ , quintupled increasing from  $4.2 \text{ pA}$  to  $20 \text{ pA}$  as the temperature increased from  $300 \text{ K}$  to  $310 \text{ K}$ . The current at the drain to gate junction of the SiC JFET, under the same biasing conditions, remained negligible at  $310 \text{ K}$  (as it was at  $300 \text{ K}$ ), resulting in a white parallel ENC less than  $1 \text{ e}^- \text{ rms}$ .

A model for computing the equivalent noise charge contribution of the input JFET of a charge sensitive preamplifier without the feedback resistor has been presented. Given the material and geometry of the JFET (channel length, width and height), and the



doping concentration at the channel and gate, the model enabled computation of the equivalent noise charge with varied temperature, shaping time and bias condition of the JFET. Using this model, it has been shown that a JFET made of SiC has lower noise contribution compared to the same geometry JFET made of Si. This was mostly attributed to the higher gate current presented in the Si device compared to SiC at  $T=300$  K, with the latter being limited by its  $1/f$  noise. Also, the large dependence of the white parallel noise to small increments in temperature has been underlined which makes the use of a wide bandgap JFET at elevated temperatures particularly advantageous.

It should be noted here that the above results are based on analytical theory, and experimentally determined values might be different due to non-idealities in the devices. Such measurements are planned and will be reported separately in due course.

## 5. Conclusions

The parameters of the input transistor which affect the total noise of the system have been discussed in the previous sections. Input transistor capacitance,  $C_i$ , is added in the total capacitance of the input of the preamplifier,  $C_T$ , which affects the series white noise and the  $1/f$  noise contribution to the total noise. It has been shown that the input capacitance of the JFET,  $C_i$ , should match the input load capacitance,  $C_d$ , once the latter has been minimized. The input transistor capacitance is proportional to the channel length,  $l$ , and width,  $W$ . When reducing the dimensions of the gate-channel junction  $C_i$  decreases. However, as  $W$  decreases, the transconductance,  $g_m$ , is also decreased, which results in higher series white noise spectral density. In order that the transconductance be as large as possible, a relatively large width is required. When the detector capacitance dominates over the transistor capacitance, a large width, and consequently a large  $C_i$  value, does not result in significant noise increment. However, a big  $C_i$  value can be balanced by matching it to the detector capacitance. Hence, by increasing the width of the channel, the resulting increment in  $C_i$  can be regarded negligible for the capacitively matched case.

The gate current of the JFET,  $I_G$  (defined in Section 3.4), contributes to the parallel white noise, degrading the spectral resolution of the system. It is mainly formed by the leakage current of the detector,  $I_{LD}$ , except when it is very low (in the range of fA) where the FET leakage current typically dominates for Si and narrower bandgap materials. The FET itself determines the drain to gate current which comes from thermal and impact ionization of carriers in the corresponding depletion layer. It has been shown that this leakage current is reduced when  $I_{DSS}$  is chosen to be relatively small and the channel length,  $l$ , is chosen to be relatively big, which both decrease the drain current,  $I_D$ . However, large channel lengths result in higher input capacitance,  $C_i$ . Instead, it has been shown that wide bandgap semiconductor materials may be used to reduce the drain to gate leakage current compensating for a small channel length.

Having an input JFET with low input capacitance,  $C_i$ , and a high transconductance,  $g_m$ , at the desired operating point, results in a small value of the  $1/f$  parameter,  $\alpha_{1/f}$ . This has a direct effect on the ratio  $f_c/f_T$  and consequently in the  $1/f$  noise contribution. Low flicker noise requires a low  $f_c/f_T$  ratio, which is achieved with  $\alpha_{1/f}$  as small as possible.

The contribution of the input transistor to dielectric noise was also discussed. Eliminating the package of the FET by integrated the FET's die onto the detector is clearly advantageous [7] as is integrating the FET with the detector as in a DEPFET detector [27]. The latter is an achievement that is well established in Si, but it is yet to be demonstrated in SiC. Furthermore and synergistic with this, it has been shown that using a JFET made of semiconductor

materials with lower dissipation factor than Si, such as SiC, results in significant reduction of the equivalent noise charge contribution due to dielectric noise, which in some situations can set the lower limit to the system. In addition, the white parallel noise component arising from a SiC JFET was computed to be negligible compared to the white parallel noise component arising from the same geometry Si JFET at long shaping times and 300 K. The difference in their white parallel noise was found to be even bigger as the temperature further increased, making the use of SiC JFET at elevated temperatures beneficial. Experimental characterization of SiC JFETs is required in order to validate the present theoretical analysis and help demonstrate the usefulness of wide bandgap input FETs for high temperature, extreme environment X-ray spectroscopy. Such measurements are planned and will be reported separately in due course.

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## References

- [1] W.R. Leo, *Techniques for nuclear and particle physics experiments: a how-to approach*, 2nd ed., Springer-Verlag, Berlin Heidelberg, 1997.
- [2] G. Bertuccio, *IEEE Solid State Circuits Magazine* 4 (2012) 36.
- [3] S.S., Kapoor, V.S., Ramamurthy, New Age International (P) Ltd., New Delhi; 1986.
- [4] G. Bertuccio, A. Pullia, G. De Geronimo, *Nuclear Instruments and Methods in Physics Research Section A* 380 (301) (1996).
- [5] R. Lowell, M. DuBose, *Geophysical Research Letters* 32 (2005) 1.
- [6] G. Bertuccio, P. Rehak, D. Xi, *Nuclear Instruments and Methods in Physics Research Section A* 326 (1993) 71.
- [7] G. Bertuccio, L. Fasoli, C. Fiorini, M. Sampietro, *IEEE Transactions on Nuclear Science* 42 (1995) 1399.
- [8] A. Fazzi, G.U. Pignatelli, G.F. Dalla Betta, M. Boscardin, V. Varoli, G. Verzellesi, *IEEE Transactions on Nuclear Science* 47 (2000) 829.
- [9] E. Elad, *IEEE Transactions on Nuclear Science* 19 (1972) 403.
- [10] G. Bertuccio, A. Pullia, *Review of Scientific Instruments* 64 (1993) 3294.
- [11] F. Levinzon, L. Vandamme, *Fluctuation and Noise Letters* 10 (2011) 447.
- [12] G. Bertuccio, S. Caccia, *Nuclear Instruments and Methods in Physics Research Section A* 579 (2007) 243.
- [13] B.J. Sheu, D.L. Sharfetter, P.K. Ko, M.-C. Jeng, *IEEE Journal of Solid-State Circuits* 22 (1987) 558.
- [14] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. Van Langevelde, G. Smit, A. Scholten, D. Klaassen, *IEEE Transactions on Electron Devices* 53 (2006) 1979.
- [15] E. Gatti, P.F. Manfredi, M. Sampietro, V. Speziali, *Nuclear Instruments and Methods in Physics Research Section A* 297 (1990) 467.
- [16] H. Spieler, Oxford University Press, New York; 2005.
- [17] A.D., Evans, McGraw-Hill; 1981.
- [18] M.P., Norton, D.G., Karczub, 2nd ed., Cambridge University Press, UK; 2003.
- [19] R.M., Howard, John Wiley & Sons, Canada; 2002.
- [20] V. Radeka, *IEEE Transactions on Nuclear Science* 20 (1973) 182.
- [21] R., Boylestad, L., Nashelsky, 9th ed., Pearson Education, New Jersey; 2006.
- [22] F.M. Klaassen, *IEEE Transactions on Electron Devices* 18 (1971) 74.
- [23] S.M., Sze, 2nd ed., John Wiley & Sons, Canada; 1981.
- [24] F.N. Trofimenkoff, *Proceedings of the IEEE* 53 (1965) 1765.
- [25] G., Vasilescu, Springer-Verlag Berlin Heidelberg; 2005.
- [26] B.G., Lowe, R.A., Sareen, Taylor and Francis Group, US; 2014.
- [27] C. Zhang, P. Lechner, G. Lutz, M. Porro, R. Richter, J. Treis, L. Strüder, S. Nan Zhang, *Nuclear Instruments and Methods in Physics Research Section A* 568 (2006) 207.
- [28] A., Bar-Lev, 3rd ed., Prentice Hall, Hertfordshire; 1993.
- [29] A. Van der Ziel, *Proceedings of the IEEE* 51 (1963) 461.
- [30] J., Sonsky, R.N., Koornneef, L.K., Nanver, G.W., Lubking, J., Huizenga, R.W., Hollander, C.W.E., Van Eijk, *Proceedings of IEEE Nuclear Science Conference Record*, 2, 2000, 204–208.
- [31] A.M. Barnett, J.E. Lees, D.J. Bassford, J.S. Ng, *Nuclear Instruments and Methods in Physics Research Section A* 673 (2012) 10.
- [32] G. Bertuccio, R. Casiraghi, *IEEE Transactions on Nuclear Science* 50 (2003) 175.
- [33] E.S., Oxner, Marcel Dekker, New York; 1989.

- [34] G. Bertuccio, D. Puglisi, D. Macera, R. Di Liberto, M. Lamborizio, L. Mantovani, IEEE Transactions on Nuclear Science 61 (2014) 961.
- [35] A.M. Barnett, G. Lioliou, J.S. Ng, Nuclear Instruments and Methods in Physics Research Section A 774 (2015) 29.
- [36] P.G. Neudeck, S.L. Garverick, D.J. Spry, L.-Y. Chen, G.M. Beheim, M.J. Krasowski, M. Mehregany, Physica Status Solidi A 206 (2009) 2329.
- [37] J.W. Palmour, M.E. Levinshtein, S.L. Romyantsev, G.S. Simin, Applied Physics Letters 68 (1996) 2669.
- [38] M.E. Levinshtein, S.L. Romyantsev, M.S. Shur, R. Gaska, M.A. Khan, IEE Proceedings of Circuits, Devices and Systems 149 (2002) 32.
- [39] S.M., Sze, 3rd ed., John Wiley & Sons, New Jersey; 2007.
- [40] J.W., Ung, T., Karacolak, NRSN, USNC-URSI; 2013, 69–69.
- [41] (<http://www.ioffe.rssi.ru/SVA/>) (accessed on 15.01.15).